Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (currently amended) An electronic circuit arrangement ~~comprising~~ comprising:

a clock fail circuit arranged ~~for receiving~~ to receive a clock signal and ~~generating~~ to generate an error signal upon ~~the absence~~ an absence of the clock signal~~, characterized in that the electronic circuit arrangement further comprises~~; and

an asynchronous processor arranged ~~for receiving~~ to receive said error signal and to bring the electronic circuit arrangement ~~in~~ into a pre-defined state upon detection of the error signal.

2. (original) An electronic circuit arrangement as claimed in claim 1, characterized in that the asynchronous processor comprises an interrupt input for receiving the error signal and is further arranged to execute software instructions upon reception of the error signal.

3. (original) An integrated circuit comprising an electronic circuit arrangement as claimed in claim 1.

4. (original) A bus station for use in a bus system comprising an electronic circuit arrangement as claimed in claim 1.

5. (currently amended) A bus station as claimed in ~~claim 3,~~ claim 4, characterized in that the bus station is a bus station for use in a LIN bus system.

6. (currently amended) A method for bringing an electronic circuit arrangement in a predetermined state, ~~whereby the electronic circuit arrangement comprises a clock fail circuit that~~ the method comprising:

~~detects the~~ detecting an absence of a clock ~~signal and~~ signal using a clock fail circuit;

~~generates~~ generating an error signal in response~~, characterized in that the electronic circuit arrangement further comprises an asynchronous processor that~~ to the absence of the clock signal; and

~~brings~~ bringing the electronic circuit arrangement ~~in~~ into the predetermined state using an asynchronous processor within the electronic circuit arrangement.